REMARKS

The Abstract is amended to bring it into conformity with the requirement that the Abstract not exceed 150 words. No new matter is introduced by any of the amendments, and entry thereof is requested. Claims 1-22 are in the application. Reconsideration of the application, as amended, is requested.

In one aspect, Applicants' invention is directed to flip chip packaging having improved chip-to-package interconnection by solid-state bonding of the input/output pads on the integrated circuit chip with the package substrate. The solid-state bond is formed by direct mating of metal surfaces, and does not employ any particulate conductive material. Accordingly the connections are capable of carrying very high current, and display good long-term reliability as compared to ACA or ICA particulate interconnects. Moreover the solid-state bond technique does not entail a melting or flow of any interconnecting material. Accordingly the connections can be formed at very fine geometries, typically as low as 70 micrometers pitch.

In another aspect, Applicants' invention is directed to a flip chip package configured for second level interconnection to a printed circuit board by way of interconnect structures formed in the shadow of the chip, in which the space between the surface of the integrated circuit chip and the subjacent surface of the package substrate (the "fill volume") is at least partly filled with one or more fill materials each having a selected specific elastic modulus, including a lower elastic modulus material in regions of the fill volume that overlie the second level interconnect sites. The coefficient of thermal expansion and the compliancy of the package structure in the regions overlying the second level connections can be tailored to reduce potentially damaging propagation of stress generated in the second level connections on the package to features on the integrated circuit chip, and thereby extending the long-term reliability of the package and of the interconnects.

The specific points raised by the Examiner will now be addressed, beginning with the objection to the specification.

Objection to the Specification (Abstract)

The Abstract was objected to because it exceeded 150 words. The Abstract is amended herein to bring it into conformity with the word count limit, and this objection can be withdrawn.

Rejection under 35 U.S.C. § 102(e)

Claims 1, 2, 4, 5, 7 and 8 were rejected under 35 U.S.C. § 102(e) over Jimarez *et al.* US 2001/0018230 A1 ("Jimarez 0018230").

The Examiner asserted that Jimarez 0018230 discloses interconnection by "thermo-mechanical deformation of the bumps (see figure 8)" but then stated:

> The bumps are formed on the input/output pads of the integrated circuit ship by a solder bumping process (see page 3, paragraph 0058).

And the Examiner asserted that Jimarez 0018230 discloses a "thermo-mechanically treating step" by

> ... concurrently forcing the bump against the pad (force exerted by gravity or pressure by the substrate 12 mounted on substrate 42) and heating the bump and pad (bump reflowing step).

This rejection is traversed.

Solid-state connection, formed by thermo-mechanical deformation of the bump on the pad (as in Applicants' invention), is different and distinct from a reflowed solder connection (as in Jimarez). As Applicants' specification makes clear, solid-state bonding according to the invention does not entail a melting or flow of any interconnecting material.

Jimarez 0018230 describes interconnection by a solder process to form a reflowed solder connection (as the Examiner points out), and not by thermo-mechanical deformation of the bumps to form a solid-state connection, as in Applicants' invention. That is, according to Jimarez 0018230 at least one of the members to be joined is melted to form the connection. Accordingly, Jimarez 0018230 does not teach or suggest solid-state interconnection between the bumps on the chip and the bonds pads in the package substrate, as in Applicants' invention as claimed. Applicants' claim 1 recites that the "interconnection between the bumps on the integrated circuit chip and the respective bond pads on the package substrate is established by direct mating of the bump surfaces with the respective bond pads and thermo-mechanical deformation of the bumps".

Applicants' claim 7 recites bumps "having low yield strength [and] high ductility... and thermo-mechanically treating the bumps to form solid-state connections of the bumps with their respective bond pads".

Moreover, Jimarez 0018230 makes no mention of selecting material for the deformable bumps of a material "having low yield strength [and] high ductility" such that formation of the connection by thermo-mechanical deformation is possible, and does not teach or suggest applying pressure that would suffice to accomplish deformation.

Accordingly, this rejection should be withdrawn.

Claims 1, 2, 5, 7 and 8 were rejected under 35 U.S.C. § 102(e) over Pu *et al.* U.S. 6,350,669 B1 ("Pu").

The Examiner asserted that "Pu et al. discloses ... thermo mechanical deformation of the bumps (see figures 2A-2C)" and that "Pu et al. discloses ... thermo-mechanically treating the bumps 222 to form solid-state connections of the bumps 222 with their respective bond pads (see figure 2A-2C). The thermo-mechanically treating step comprises concurrently forcing the bump 222 against the pad 211 and heating the bump and pad (see figure 2C)."

This rejection is respectfully traversed. Pu is directed to bonding a BGA package to a circuit board (second level interconnect), and has nothing to do with forming an interconnect between a chip and a package substrate (first level interconnect) as in Applicants' invention.

This second-level (package-to-board) interconnect according to Pu is made by a solder-reflow process, using two groups of solder balls having different reflow collapse degrees. As pointed out above, and as Applicants' specification makes clear, solid-state connection, formed by thermo-mechanical deformation of the bump on the pad (as in Applicants' invention), is different and distinct from a reflowed solder connection (as in Pu). Pu does not teach anything at all about first-level interconnect between flip chip and package substrate; and even as to BGA second-level connection between package substrate and circuit board, Pu does not teach or suggest solid-state interconnection, as in Applicants' invention as claimed.

Accordingly, this rejection should be withdrawn.

Claims 1, 5, 9-11, 13-16, 18 and 19-21 were rejected under 35 U.S.C. § 102(e) over Jimarez *et al.* U.S. 6,191,952 B1 ("Jimarez '952").

The Examiner asserted that Jimarez '952 "discloses ... thermo-mechanical deformation of the bumps (see figure 3)" and further that in Jimarez '952 the "thermo-mechanically treating step comprises concurrently forcing the bump against the pad and heating the bump and pad (see column 2, lines 60-63)."

As for Applicants' invention directed to the patterned fill materials in the fill volume, the Examiner asserted that Jimarez '952 "discloses ... the fill volume being at least partly filled with at least one fill material, each said fill material having a selected specific elastic modulus, wherein regions 68 of the fill volume that overlie the second level interconnect sites contain a lower specific elastic modulus fill material", and further that:

> The fill volume includes a first fill zone 68 comprising a plurality of generally columns, generally overlying the plurality of second level interconnect sites; and the second fill zone 48 consists of the remainder of the fill volume (see figure 3).

And as to Applicants' invention directed to methods for forming the patterned fill materials in the volume, the Examiner asserted that Jimarez '952 "discloses ...

These rejections are traversed.

Regarding thermo-mechanical formation of solid-state interconnects, Jimarez '952 describes solder reflow interconnection and, accordingly, Jimarez '952 fails to teach or suggest this aspect of Applicants' claimed invention.

Regarding the patterned fill materials, Jimarez '952 describes a laminate of fill materials (*e.g.*, 68, 48 in Jimarez '952 Fig. 3), and, to the extent they may be seen as "patterned" the pattern is necessarily formed in relation to the first level interconnect balls (16 in Jimarez '952 Fig. 3). According to Applicants' invention, the fill materials are patterned in relation to the second-level interconnect sites. Jimarez '952 does not teach or suggest any relationship whatever between a pattern of material[s] in the fill volume and the second-level interconnect sites, as in Applicants' claimed invention.

Accordingly, these rejections should be withdrawn.

Rejection under 35 U.S.C. § 103(a)

Claims 3 and 6 were rejected under 35 U.S.C. § 103(a) for obviousness over Jimarez 0018230. The Examiner acknowledged that Jimarez 0018230 does not teach forming the

bumps of gold or a gold alloy material, or forming the bumps on the input/output pads of the integrated circuit chip by an electroplating process", but argued that:

> With respect to forming the bumps of gold or a gold alloy material, the particular type of material used to make the bumps, is only considered to be the use of a "preferred" or "optimum" material out of a plurality of well-known materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation based, among other things, on a desire costs and product reliability.

This rejection is traversed. First of all, as noted above, Jimarez 0018230 does not teach or suggest solid-state interconnect by thermo-mechanical deformation of the bumps, and so Applicants' claimed combination is not made out in any event. Jimarez 0018230 teaches solder reflow connection, entailing melting the bumps. Accordingly, gold would not be suggested as a "preferred" or "optimum" material -- or as a candidate material at all for use in Jimarez 0018230, in view the impracticably high melting point of gold.

Accordingly, this rejection should be withdrawn.

Claims 2-4, 6-8, 12 and 22 were rejected under 35 U.S.C. § 103(a) for obviousness over Jimarez '952. The Examiner acknowledged that Jimarez '952 does not teach "an optimum preferred material selected to provide low yield strength, high ductility, and an oxidation- and corrosion-resistant bump surface, e.g. gold, for forming the solder bumps" or "different process of forming the solder bumps, e.g. electroplating or stud bumping" or a specific elastic modulus of less than about 0.5 Gpa for the first fill material".

These rejections are traversed.

As to bump materials and bump formation, as noted above, Jimarez '952 does not teach or suggest solid-state interconnect by thermo-mechanical deformation of the bumps, and so Applicants' claimed combination is not made out in any event. Jimarez '952 teaches solder reflow connection, entailing melting the bumps. Accordingly, gold would not be suggested as a "preferred" or "optimum" material -- or as a candidate material at all for use in Jimarez '952, in view the impracticably high melting point of gold. Moreover, the qualities of low yield strength and high ductility are not relevant to melting and, accordingly, selection of materials according to these criteria would not be appropriate for use in Jimarez '952.

As to elastic modulus of fill materials, as noted above, Jimarez '952 does not teach or suggest any relationship whatever between a pattern of material[s] in the fill volume and the second-level interconnect sites, as in Applicants' claimed invention, and so Applicants' claimed combination is not made out in any event. No amount of experimentation, routine or otherwise, with different materials in the fill volume configuration of Jimarez '952, would result in Applicants' claimed invention.

Accordingly, these rejections should be withdrawn.

Claims 9-11 and 17 were rejected under 35 U.S.C. § 103(a) for obviousness over Akram *et al.* U.S. 5,956,605 ("Akram") in view of Jimarez '952. The Examiner acknowledged that Akram does not teach "interconnection sites arranged in a second surface of the package substrate underlying the void spaces and second level interconnect structures connected to the respective second level interconnect sites", and argued that it would have been obvious:

> ... to disclose second interconnection sites arranged in a second surface of the package substrate 42 underlying the void spaces and second level interconnect structures connected to the respective second level interconnect sites, as disclose in Jimarez et al. in the primary reference of Akram at al. since Akram et al. suggest pads being in communication with conductive traces on or within substrate 42 (see column 7, lines 1-10).

This rejection is traversed. No combination of Jimarez '952 with Akram makes Applicants' claimed invention, as neither Akram nor Jimarez '952 (see above) teaches or suggests patterning the fill material[s] in relation to the second-level interconnect sites, as in Applicants' claimed invention.

Accordingly, this rejection should be withdrawn.

In view of the foregoing, it is believed that all the claims in the application are in condition for allowance, and action to that effect is requested.

This response is being filed within the third month following the shortened statutory period set by the Examiner, and, accordingly, it is accompanied by a petition for three months' extension of time and a fee or fee authorization therefor. In the unlikely event that the petition or fee may

become separated from this paper, petition is hereby made therefor, and the Commissioner is authorized to charge the fee to Deposit Account 50-0869 (Order No. CPAC 1008-2).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

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Attachment under Rule 1.121
(Specification)

The Abstract is amended as follows:

A flip chip package is formed by a solid-state bond technique for connecting the input/output pads on the integrated circuit chip and the package substrate. The solid-state bond technique involves a direct mating of metal surfaces, and does not employ any particulate conductive material[. Accordingly the connections are capable of carrying very high current, and display good long-term reliability as compared to ACA or ICA particulate interconnects. Moreover the solid-state bond technique does not entail a] nor any melting or flow of any interconnecting material. Accordingly the connections can be formed at very fine geometries[, typically as low as 70 micrometers pitch. Also]. In another aspect, the space between the surface of the integrated circuit chip and the subjacent surface of the package substrate is filled with a patterned adhesive structure, which consists of one or more adhesive materials that are deployed in a specified pattern in relation to the positions of the second level interconnections between the package and the printed circuit board. [According to this aspect of the invention, the coefficient of thermal expansion and the compliancy of the package structure in the regions overlying the second level connections can be tailored to reduce potentially damaging propagation of stress generated in the second level connections on the package to features on the integrated circuit chip, and thereby extending the long-term reliability of the package and of the interconnects.]